S/N 10/763,512 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christopher Lapkowski	Examiner: Tuan A Vu
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Title:	PAIRING OF SPILLS FOR PARALLEL REGISTERS	
Assignee:	International Business Machines Corporation	

PROPOSED AMENDMENTS FOR ENABLING EXAMINER'S AMENDMENT

Applicant proposes the following amendments for the limited purpose assisting the Examiner with entry of an Examiner's Amendment. Please amend the claim numbers, as needed.

1. A method of handling register spills in a CPU having parallel registers, said parallel registers including a first register set and a second register set, the method comprising:

   (i) determining that register spill instructions in spill code generated by a register allocator can be paired, ~~associated with each other,~~ wherein paired register spill instructions relate to corresponding register locations in each of the first register set and the second register set and that no instructions between said register spill instructions modify any of said register spill instructions;

   (ii) based on the determining, ~~rewriting~~ modifying said register spill instructions as a parallel register spill instruction; and

   (iii) based on said ~~rewritten~~ modified parallel register spill instruction, configuring storage of associated register spills in memory in such a manner that said register spills can be loaded ~~back~~ into said first and second register sets ~~registers~~ in parallel, wherein the configuring includes allocating space on a memory stack such that paired register spills are double word aligned.

~~2. The method of claim 1, wherein said CPU having parallel registers includes a first register set and a second register set, and wherein (i) includes determining that two register spill instructions can be paired.~~

3. The method of claim 1, wherein (i) includes determining that said register spill instructions are in a basic block within said spill code.

~~4. The method of claim 1, wherein (i) includes determining that said register spill instructions relate to matching register locations in each of a first register set and a second register set.~~

~~5. The method of claim 1, wherein (i) includes determining that no intervening instructions between said register spill instructions modify any of said register spill instructions.~~

6. The method of claim 1 [[2]], wherein (iii) includes ~~first allocating space on a memory stack to all paired register spills, then~~ allocating space on said memory stack for any remaining register spills.

~~7. The method of claim 2, wherein (iii) includes allocating space on said a memory stack such that paired register spills are double-word aligned.~~

8. The method of claim [[7]] 1, further comprising loading said paired register spills ~~spill instructions~~ from said memory stack back into ~~matching~~ corresponding register locations in each of said first register set and said second register set in parallel.

9. A system for handling register spills, the system including ~~in~~ a CPU having parallel registers including a first register set and a second register set, the system comprising:
(a) an analyzer module configured to analyze spill code generated by a register allocator to determine that register spill instructions can be paired, wherein paired register spill instructions relate to corresponding register locations in each of the first register set and the second register set and that no instructions between said register spill instructions modify any of said register spill instructions;
(b) a rewriter module configured to, based on the determining, ~~rewrite~~ modify said register spill instructions as a parallel register spill instruction; and
(c) a storage module configured to configure storage of associated register spills in memory in such a manner that said register spills can be loaded back ~~into said registers~~ in parallel into corresponding registers of said first and second register

sets based on said ~~rewritten~~ modified parallel register spill instruction, wherein the configuration of storage includes allocation of space on a memory stack such that the register spills are double word aligned.

~~10. (Currently Amended) The system of claim 9, wherein said CPU having parallel registers includes a first register set and a second register set, and said analyzer module in (a) is configured to determine whether that two register spill instructions can be paired.~~

11. The system of claim 9, wherein said analyzer module in (a) is configured to determine that said register spill instructions relate to matching register locations in each of a first register set and a second register set.

~~12. The system of claim 9, wherein said analyzer module in (a) is configured to determine that no intervening instructions between said register spill instructions modify any of said register spill instructions.~~

13. The system of claim 9 [[10]], wherein said storage module in (c) is configured to first perform the allocation of ~~allocate~~ space on [[a]] the memory stack to all paired register spills, then to allocate space on said memory stack for any remaining register spills.

~~14. The system of claim 10, wherein said storage module in (c) is configured to allocate space on said a memory stack such that paired register spills are double word aligned.~~

15. The system of claim 9 [[14]], wherein the storage module is further configured to load ~~comprising loading~~ said paired register spills from said memory stack back into matching register locations in each of said first register set and said second register set in parallel.

16. A system for handling register spills in a CPU having parallel registers, said parallel registers including a first register set and a second register set; said system comprising:

(a) means for determining that register spill instructions in spill code generated by a register allocator can be paired, wherein paired register spill instructions relate to corresponding register locations in each of the first register set and the second

register set and that no instructions between said register spill instructions modify any of said register spill instructions; ~~associated with each other;~~

(b) means for, based on the determining, ~~rewriting~~ modifying said register spill instructions as a parallel register spill instruction;

(c) means for configuring, based on said modified~~rewritten~~ parallel register spill instruction, storage of associated register spills in memory in such a manner that said register spills can be loaded ~~back~~ into said first and second register sets ~~registers~~ in parallel, wherein the configuring includes allocating space on a memory stack such that paired register spills are double word aligned.

~~17. The system of claim 16, wherein said CPU having parallel registers includes a first register set and a second register set, and wherein (a) includes means for determining whether two register spill instructions can be paired.~~

~~18. The system of claim 16, wherein (c) includes means for allocating space on said a memory stack such that paired register spills are double word aligned.~~

19. The system of claim 16, further comprising means for loading said paired register spills from said memory stack back into matching register locations in each of said first register set and said second register set in parallel.

20. A computer readable storage medium having computer readable program code for handling register spills in a CPU having parallel registers, said parallel registers including a first register set and a second register set, the computer readable program code comprising:

(i) code for determining that register spill instructions in spill code generated by a register allocator can be paired, wherein paired register spill instructions relate to corresponding register locations in each of the first register set and the second register set and that no instructions between said register spill instructions modify any of said register spill instructions; ~~associated with each other;~~

(ii) code for modifying ~~rewriting~~, based on the determining, said register spill instructions as a parallel register spill instruction;

(iii) code for configuring, based on said rewritten parallel register spill instruction, storage of associated register spills in memory in such a manner that said register spills can be loaded back into said first and second register sets ~~registers~~ in parallel, wherein the configuring includes allocating space on a memory stack such that paired register spills are double word aligned.

~~21. The computer useable medium of claim 20, wherein said CPU having parallel registers includes a first register set and a second register set, and wherein (i) includes code for determining whether two register spill instructions can be paired.~~

~~22. The computer useable medium of claim 21, wherein (iii) code for allocating space on a memory stack such that paired register spills are double word aligned.~~

23. The computer ~~useable~~ readable storage medium of claim 20 [[22]], the computer readable program code further comprising code for loading said paired register spills from said memory stack back into matching register locations in each of said first register set and said second register set in parallel.

Respectfully submitted,

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